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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 4 : C23C 16/44 — A1

(11) International Publication Number: WO 90/04045

(43) International Publication Date: 19 April 1990 (19.04.90)

(21) International Application Number: PCT/US89/04592

(22) International Filing Date: 13 October 1989 (13.10.89)

(30) Priority data:
257,854 — 14 October 1988 (14.10.88) — US
257,855 — 14 October 1988 (14.10.88) — US

(60) Parent Applications or Grants
(63) Related by Continuation
US 257,854 (CIP)
Filed on 14 October 1988 (14.10.88)
US 257,855 (CIP)
Filed on 14 October 1988 (14.10.88)

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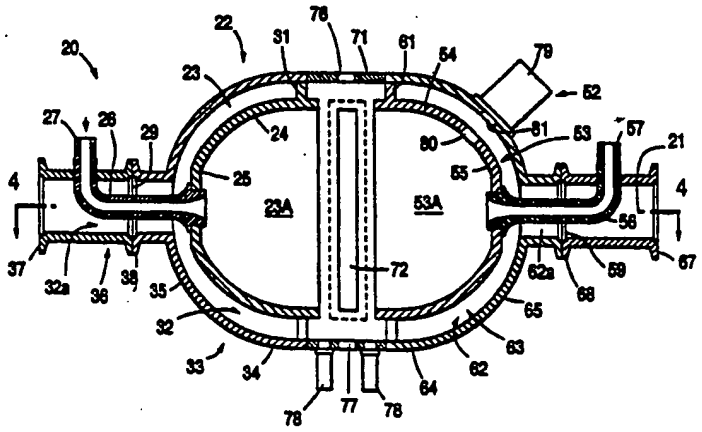
(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent), US.

Published
With international search report.

(54) Title: SEMICONDUCTOR WAFER PROCESSING METHOD AND APPARATUS



(57) Abstract

A semiconductor wafer processing method and apparatus are disclosed with a processing housing (20) having a substantially horizontal axis with support structure (71) for at least one wafer on the axis and a housing member (33, 63) and method of introducing and directing a treatment medium substantially parallel to the horizontal axis and withdrawing that medium coaxial with the directed treatment medium. The apparatus includes a pair of coaxial hollow cylindrical members (23, 53) defining an inner cylindrical chamber (23A, 53A) for directing the treatment medium toward the wafer and an annular chamber (32, 62) for withdrawing the treatment medium. A support structure (71) which can include a heater will support one or two wafers in the apparatus. A treatment medium is introduced in vapor phase at very low to high velocity and at subatmospheric to superatmospheric pressure. Radiation (79) can be introduced into the housing, and wafers can be automatically moved into and out of the housing and from the housing to another wafer treating apparatus. The process includes evacuation desorption steps before and after the treatment step.

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SEMICONDUCTOR WAFER PROCESSING METHOD AND APPARATUS

This invention relates in general to semiconductor integrated circuit (IC) wafer processing method and apparatus and more particularly to method and apparatus for automation of various fabrication steps in the semiconductor IC wafer fabrication process. This application is a continuation-in-part of co-pending applications Serial Nos. 257,854 and 257,855, filed October 14, 1988 of the same title which are continuations-in-part of application Serial No. 919,313, filed October 15, 1986, entitled "Semiconductor Substrate Heater And Reactor Process And Apparatus", now Patent No. 4,778,559 issued October 18, 1988.

BACKGROUND

As semiconductor IC fabrication processing has developed, different wafer processing treatments have developed such as, for example, diffusion, oxidation, metalization, chemical vapor deposition (CVD) of thin films like epitaxial silicon and dielectric depositions like silicon dioxide and silicon nitride and ion implantation. Many of these treatments required heating of the wafer during treatment and removal of surface contaminants on the wafer before and/or after the treatments. Different methods and increasingly complicated physical structures have been developed and used for different treatments thereby complicating the semiconductor fabrication process, requiring more handling by personnel typically introducing contamination, increasing the time and space utilized in producing integrated circuits and often decreasing the yield and product reliability.

Since the integrated circuit was first developed the complexity of the circuits has increased and the circuits have become more closely packed and more densely wired. The size of wafers on which the integrated circuits are made has steadily increased up to a current eight inches in diameter, and in many devices the processing steps have greatly increased in number. In 1983 a 64K (DRAM) Dynamic Random-Access-Memory device was manufactured on a four inch wafer with a minimum feature size of 2.5 to 4.0 micrometers using 132 process steps with 7 chemical vapor deposition steps and typically 18 wet chemical cleaning steps. Defects as small as 0.5 microns can have catastrophic effects on yield, and these defects can be caused by particulate contamination and/or defects in the thin films. Today a 4 MEG DRAM utilizes in excess of 250 process steps, a minimum feature size of less than 1.0 micrometers, in excess of 12 CVD process steps and more than 50 cleaning steps. The newer devices require less contamination, and people and chemicals contribute heavily to the contamination of semiconductor wafers.

Traditionally, chemical cleaning of wafers has involved immersion in a vat of hazardous chemicals in aqueous solution using a "wet deck" for a set amount of time. The wafers are removed from the bath, rinsed and spun dry. This sequence results in additional processes and handling steps, dilution of the bath and contamination of the device wafer due to exposure to air after each step. Scrubbing using brushes or high pressure fluid jets has been used in these wet processes. Newer cleaning processes have included centrifugal spraying and use of liquids flowing past the wafers.

Traditional wafer cleaning processes are not effective for removing contaminants in the

manufacture of devices with a critical feature size of 3 microns or less. Cleaning chemistries in the liquid phase cannot reach into many miniaturized crevices and troughs typical of the geometry in the new generation of integrated circuits. After a wafer has been submerged in an industry-standard wet deck containing liquid cleaning chemistry, a droplet, influenced by surface tension, rests on top of the trough unable to remove contaminates in the trough and can deposit particulates and other contaminates there.

Environmental contamination and personnel hazards are additional major problem created by existing wet deck cleaning systems. The highly corrosive chemicals commonly used in traditional wet deck cleaning have proven to be hazardous to people and the environment.

A major source of contamination occurs in movement and storage of wafers from many of the processing steps into inventory of the partially processed wafer requiring individual cleaning steps before many of the subsequent treatment steps. This periodic movement of the wafer into and out of inventory adds to the chance of contamination and consequently reduced yield and contributes greatly to the expense of the equipment and manufacturing space required for producing a completed wafer.

With larger wafers and smaller critical feature sizes uniform heating of the wafer during the treatment steps has become more important. RF heating and radiant energy heating have been utilized. RF generators and infrared lamps are expensive to manufacture and maintain as well as large in size, thereby consuming large areas of expensive floor space and power. The batch processing with these equipments added to the expense

and potential contamination of IC fabrication. Still, these processes have resulted in non-uniformity of heating, especially with the larger diameter wafers being used to manufacture certain integrated circuits, and the methods and apparatus used for heating the wafer inhibited integration and automation of the various steps in fabrication of a semiconductor device wafer.

SUMMARY OF THE INVENTION

The object of the present invention is to provide method and apparatus for fabricating semiconductor device wafers and which reduce time, expense and hazards in production and increase the product quality and yield.

Broadly stated the present invention is directed to semiconductor device wafer processing method and apparatus wherein the wafer is handled in treatment apparatus and/or steps positioned in a substantially vertical position and moved automatically from one treatment apparatus or step to the next.

One aspect of the present invention includes the provision of method and apparatus for positioning the semiconductor wafers substantially vertically, directing a treatment medium, such as a cleaning and/or reactant substance, substantially horizontally perpendicularly against at least one face of the wafer and withdrawing the treatment medium away from the face of the wafer substantially coaxially around and outwardly from the treatment medium being directed against the face of the wafer.

A feature and advantage of the invention is that this method and apparatus enables sequential integration and automation of known processes.

In accordance with another aspect of the present invention, method and apparatus are provided for

establishing a substantially vertical wafer treating position and directing a treatment medium, such as cleaning or reactant substance, simultaneously, substantially horizontally in one direction or opposite directions against the wafer treating position and withdrawing the treatment medium away from the wafer treating position coaxially and outwardly from the medium being directed against the wafer treating position.

A feature and advantage of this aspect of the present invention is the ability to perform or position sequential treatment and/or cleaning and/or processing steps or apparatus closely spaced from one another whereby the wafer can be transferred from one apparatus or processing stage to the next, thereby minimizing potential contamination of the wafer and the amount of manufacturing space required for processing the wafer.

In accordance with another aspect of the present invention the processing apparatus comprises means for supporting at least one wafer substantially vertically at a wafer treating position along the horizontal axis of a processing housing, a first housing member centered on the housing horizontal axis on one side of the wafer treating position, means for introducing and directing a treatment medium in the form of a cleaning or reacting gas or vapor into the housing in a direction substantially parallel to the horizontal axis and toward and against the wafer treating position. A second housing member centered on the housing horizontal axis is provided with means for introducing and directing a treatment medium into the second housing in a direction substantially parallel to the horizontal axis and toward and against the wafer treating position in a direction opposite the

direction of the treatment medium in the first housing member.

A feature and advantage of the invention is that at the wafer treating position either one or both sides of a wafer can be treated or one side of each of a pair of wafers can be treated simultaneously either similarly or differently.

In accordance with still another aspect of the present invention the treatment medium is introduced into the housing member in vapor phase.

In accordance with still another aspect of the present invention the treatment medium is directed for very low velocity or high velocity impingement upon the face of a wafer at the wafer treating position for treating the surface of the wafer and/or dislodging particles from the surface of the wafer.

In accordance with still another aspect of the present invention method and apparatus are provided whereby a wafer can be heated uniformly across the wafer.

In accordance with still another aspect of the present invention methods and means are provided for introducing radiation such as ultraviolet, infrared, and coherent light into the housing for use in the treatment of the wafer.

In accordance with still another aspect of this invention the method includes evacuation steps before and after the treatment step for desorption and evacuation of gases and condensate including reaction products.

In accordance with the next preceding aspect of this invention, an additional aspect of the invention is an evacuation step to substantially 10^{-3} Torr after the treatment step.

These and other features and advantages of the present invention will become more apparent upon a perusal of the following specification taken in conjunction with accompanying drawing wherein similar characters of reference identify similar structure in each of the several views.

DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic block diagram view of the first seven steps in a current prior art manufacturing process for a 64K DRAM IC.

Figure 2 is a schematic elevational view, partially in broken away and partially in block diagram form, illustrating the method and apparatus of the present invention.

Figure 3 is a side elevational, sectional view of a portion of the structure shown schematically in Figure 2.

Figure 4 is a sectional view of the structure illustrated in Figure 3 taken along line 4-4 in the direction of the arrows.

Figure 5 is a schematic flow diagram illustrating a use and operation of the structure illustrated in Figures 3 and 4.

Figure 6 is an elevational view of a wafer illustrating the uniformity of a wafer surface layer after partial removal of a silicon dioxide layer generally utilizing the structure of Figure 3 and 4.

Figure 7 is a side elevational sectional view of an alternative embodiment of a portion of the structure illustrated in Figure 2.

Figure 7A is an alternative embodiment of a portion of the structure shown in Figure 7.

Figure 8 is a schematic, elevational view, partially broken away and partially in line form, illustrating another embodiment of the present invention.

Figure 9 is a graph of pressure plotted against time for the process chamber of Figure 8 for a cycle for hydrogen fluoride water vapor-phase etching of thermal oxide.

Figures 10A and 10B are graphs plotting oxide thickness versus distance across a wafer wherein

Figure 10A shows the thermal oxide thickness before and after a vapor-phase HF etching and Figure 10B shows the total oxide etched.

Figure 11 is a graph of oxide thickness plotted versus etch time for etching SiO_2 in vapor-phase HF/H_2O.

Figure 12 is a graph of oxide thickness versus etch time for etching of borophosphosilicate glass film in vapor-phase HF/H_2O.

Figure 13 is a schematic side elevational view, partly in section, illustrating the mechanism involved in vapor-phase HF etching of an oxidized silicon wafer.

Figure 14 is a graph of native oxide thickness plotted versus time showing the regrowth of "native" oxide on a silicon wafer after removal of oxide in vapor-phase HF/H_2O.

Figure 15 is a schematic elevational view, partially in section of an integrated processing system incorporating the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

While the present invention is applicable to various aspects of methods and apparatus for processing semiconductor wafers, the invention is specially applicable to the production of integrated circuits through the treatment of semiconductor wafers, such as cleaning and surface processing of wafers which may include heating, etching, reacting and/or cleaning, in independent steps as well as in sequential integrated processing steps. The invention will be described with respect to a small number of steps performed in the processing of semiconductor wafers for integrated circuit manufacture.

Referring now to Figure 1 there are shown the first 7 steps in a current state of the art or prior art manufacturing process for a 64K dynamic random-access memory (DRAM) IC device. Seven processing steps are shown beginning with inspection of the wafer at stage 1, following which the wafer is cleaned in step 2 and sent to inventory. In the third processing step the wafer is removed from inventory and an epitaxial EPI layer is grown on the wafer and the wafer returned to inventory. Before further processing the wafer is removed from inventory and run through a cleaning step 4 and returned to inventory. the wafer is removed from inventory for the fifth step which is shown as growing an initial oxide, and the wafer is then returned to inventory. Next, preparatory for further processing the wafer is removed from inventory and cleaned in step 6 and returned to inventory. Finally the wafer is removed from inventory and processed in the seventh step which is illustrated as a chemical vapor deposition (CVD) of silicon nitride. Following the seventh step the wafer is sent on to a lithograph step.

In accordance with the present method and apparatus the wafer can be sequentially processed with the apparatus schematically illustrated in Figure 2, wherein the wafer is directed into an assembly 10 including a cleaning apparatus 13, such as for growing an EPI layer and directly into a further processing apparatus 17, such as for providing a CVD processing step such as the initial oxide. The seven steps shown in Fig. 1 are reduced to a processing treatment in an integrated processing apparatus which is adaptable to performing different functions. Wafers are introduced into the assembly 10 typically in wafer carriers 11 and individually

automatically conveyed to the cleaning apparatus 12, treatment apparatus 13 and processing apparatus 17 from which they are removed and carried on for further steps in the manufacturing process in the wafer cassette 11. Figure 2 schematically illustrates the utilization of appropriate processing treatment media and/or materials or reactants in the containers generally designated 18 which are appropriate for the particular step being carried on at the appropriate stage of the manufacturing process. If an independent cleaning step is required between the treatment step performed in treatment apparatus 13 and the processing step performed in the processing apparatus 17, a supplementary cleaning apparatus 12 can be inserted between the treatment apparatus 13 and the processing apparatus 17.

Referring now to Figure 3 and 4 there are shown a side elevational sectional view and a horizontal sectional view, respectively, of a portion of the cleaning apparatus 12 which includes a processing housing 20 having a substantially horizontal axis along the sectional line 21 in Figure 3. The housing 20 takes the form of a pair of reaction of cleaning hollow belljar shaped chambers on each of the opposite sides of a substantially vertical support position for semiconductor wafer(s). Processing media are directed from opposite horizontal directions to the wafer position.

The processing housing 20 includes a first housing member 22 having an inner cup shaped wall 23 made of a non-contaminating material such as Teflon or silicon carbide and which includes a hollow cylindrical portion 24 open at one end and closed at the cup shaped end by a hemispherical portion 25.

The inner wall 23 is coaxially mounted within a similarly shaped outer cup shaped wall 33 which has

hollow cylindrical and spherical portions 34 and 35 similar to but larger than the hollow cylindrical and spherical portions 24 and 25. Hollow cylindrical portion 24 includes a plurality of radially outwardly projecting spacer portions or members 31 positioned in the annular space 32 between the cylindrical portions 24 and 34 of the walls 23 and 33 for maintaining the walls in coaxially spaced apart position, and the spacer members 31 permit flow of media such as gas or vapor in the space between the walls 23 and 33.

Inner and outer coaxial tubular members 26 and 36 are provided to the center of the hemispherical portions 25 and 35, respectively. These tubular members 26 and 36 are maintained in coaxial spaced apart relation by an apertured annular spacer 29, such as of teflon, positioned in the annular space 32a between the tubular members 26 and 36 at a flanged joint 38 in the tubular member 36. Tubular member 26 bends and exits through an aperture in tubular member 36 to an inlet end 27. Tubular member 36 extends to an outlet end 37. The outer wall 33 and its connecting tubular member 36 are made of an inert material such as silicon carbide or teflon. The outlet end 37 of the tubular member 36 provides exit communication from the annular space 32a between the tubular members 26 and 36 and, therefore, exit from the annular space 32 between the inner and outer walls 23 and 33.

Spaced from and facing the open end of the first housing member 22 is a second housing member 52 which includes inner and outer wall members 53 and 63, respectively, shaped similar and connected to parts shaped similar to those connected to inner and outer wall members 23 and 33, respectively. The second housing member includes parts identified in the

drawings with reference numbers in the number ranges in the 50's and 60's having digits corresponding to similarly constructed parts described above with reference numbers in the 20's and 30's.

The open ends of the outer cylindrical wall portions 34 and 64 of the first and second housing members 22 and 52, respectively, are connected to opposite sides of an annular ring 71 which has a dimension in the horizontal axial direction of the processing housing 20 such that the open ends of the inner walls 23 and 53 of the first and second housing members 22 and 23 are spaced apart so that semiconductor wafers can be positioned for treatment therebetween in a wafer treating position 72 with chambers 23A and 53A on opposite sides thereof within the respective inner wall members 23 and 53. Annular ring 71 has a vertically oriented, elongate, lateral extension 73 provided on the outer end thereof with a flange 74 for mounting a load/unload gate valve (not shown) for introducing wafers into and removing wafers from the wafer treating position 72 through a vertical passageway 75 in extension 73.

The inlet ends 27 and 57 of tubular members 26 and 56, respectively, enable injection of suitable media into chambers 23a and 53a in a direction substantially parallel to the horizontal axis 21 and toward the wafer treating position 72 to clean or treat opposite sides of a semiconductor wafer located at the wafer treating position 72 or a single side of each of a pair of wafers that are positioned on a heating assembly such as that illustrated in Figure 7 and described below. The media introduced on the horizontal axis of the processing housing 22 are vacuum drawn out of the housing 22 through the annular spaces 32-32a and 62-62a surrounding and coaxial with introduced media. This construction

provides for application of the media uniformly across the surface of the wafer.

Wafer injection and transporting structure, such as automatically controlled robotic mechanisms, can move vertically oriented wafers either laterally into the cleaning apparatus 12 as shown in the apparatus of Figures 3 and 4 or through the cleaning apparatus 12 as schematically illustrated in Figure 2 or vertically into and out of the processing housing 20.

The top and bottom portions of the annular ring 71 are apertured at 76 and 77, respectively, for actuating members (not shown), such as pairs of solenoid operated gripping fingers, for gripping the wafer which has been moved into the wafer treating position 72 by the wafer injecting and transporting structure.

A pair of light sources 78 can also be positioned on the opposite sides of the aperture 77 on the bottom of annular ring 71 to provide a beam immediately adjacent the wafer surface.

A radiation source 79, such as a ultraviolet or infrared source, a broadband source or a coherent light source from a lamp, filament, laser or plasma discharge, is positioned on one or both of the housing members 52 and 22 for transmission of radiation through appropriate windows 80 and 81 in inner and outer walls 55 and 65 into the chambers 53A and 23A for providing radiation desired for a reaction in the chambers 53A and 23A.

In accordance with this invention a semiconductor wafer or pair of wafers are moved into the wafer treating position and treated such as with a cleaning or reacting medium injected into the chambers 23A and 53A from the inlets 27 and 57. The treating media from chambers 23A and 53A are respectively withdrawn coaxially with respect to the

media being introduced and through the annular spaces 32-32a and 62-62a and outlets 37 and 67. The wafer surfaces facing the chambers 23A and 53A can be treated the same, such as with the same medium, or differently, such as with a different treatment medium. If desired a diffuser plate (not shown) can be positioned in each of the chambers 23A and 53A for diffusing and distributing the medium injected therein for more uniform application to the face of the wafer.

The treatment apparatus 13 shown in Fig. 2 can take the same physical configuration as the processing housing 20 shown in Figures 3 and 4 and appropriate reactants introduced and directed to the appropriate wafer surface to grow the EPI layer.

A semiconductor wafer processing method and apparatus in accordance with the preferred embodiment of this invention as illustrated in Figures 3 and 4 has a processing housing 20 with inner walls 23 and 53 having an inside diameter of 7 inches and axial length of 8 inches and outer walls 33 and 63 having an inside diameter of 9 inches. This apparatus will process 6 inch diameter wafers with flow rates of the media from I cc to 100 I. per minute and possible chamber pressures over the range from 10^{-8} Torr to 250 psi. Using this diameter apparatus or larger to accommodate larger wafers this method and apparatus will process in the range of 30 to 180 five inch to twelve inch diameter wafers per hour.

An illustrative example of vapor phase hydrogen fluoride (HF) etching of silicon dioxide utilizing the present invention is provided in Figure 5. As shown there, a cleaning apparatus 12 in accordance with the present invention is supplied at the inlet ends 27 and 57 for chambers 23A and 53A with vapor phase media from a line 211 from a mixing block 212

which receives media from either a vapor HF heated line 220, a steam heated line 230 and/or a purge nitrogen (N_2) line 240.

For the vapor HF line 220 a N_2 carrier 221 is passed through a line 221a to a mass flow controller 222 and then via a line 222a and appropriate valving either to a HF source 223, a mass flow controller bypass to exhaust 224 or a purge line 225 bypassing the HF source 223. The HF source 223 is an aqueous solution of HF and H_2O. A sizeable volume of HF-H_2O mixture is kept in a plastic container immersed in a constant temperature heating bath 226 and stirred by a magnetic stirrer 227. The nitrogen carrier gas 221 is passed over the surface of the HF-H_2O liquid at a constant flow rate. The N_2-H_2O-HF mixture exiting the source 226 is passed through an insulated teflon tubing 228 that is heated to at or above the temperature of the liquid so as to prevent condensation in the tubing. The steam in steamline 230 is generated from deionized water in a reservoir 231 through a line 231a to a pressure regulator 232 such as a high pressure relief valve (40-150 psi) and via line 232a through appropriate valving and a submicron filter 233 and to and through a super heated steam generator 234 heated by heaters 235 in a insulated chamber 236. The steam is carried through an insulated and heated tubing 237 to the mixing block 212.

Nitrogen (N_2) used for a system purge or a micro rinse drying cycle from a N_2 source 241 is conveyed via line 241a through a mass flow controller 242 and then via line 242a through the chamber 236 wherein the temperature of the nitrogen can be controlled via the temperature control 243 for passage through line 240 to the mixing block 212 and the cleaning apparatus 12.

Flow control of the media through the cleaning apparatus 12 is established in the exhaust assembly which includes exhaust line 250a connected to the outlet ends 37 and 67 and in turn directed to a particulate filter 251 connected in turn via line 251a to a vacuum pump 252. The exhaust from vacuum pump 252 is passed via line 252a first through an acid trap 253 and then a base trap 254 to the facility exhaust.

The automated process utilizing the cleaning apparatus 12 includes (a) a first step of pressurizing the chamber of the cleaning apparatus 12 to a positive pressure such as with N_2 from line 241, (b) opening the load/unload valve, (c) loading and positioning the wafer in the chamber, (d) closing the load/unload valve, (e) evacuating the chamber to approximately 10^{-3} Torr, (f) heating the wafer to processing temperature if required, (g) adjusting the chamber pressure to the processing level and selecting the appropriate programmed process sequence.

For HF removal of oxides the sequence includes (h) directing the desired amount of HF and an amount of steam, if required, to the mixing valve 212 (i) turning the HF off, (j) directing only N_2 carrier gas to the chamber, (k) pumping the system to purge the chamber to about 20 Torr, (I) back-filling the chamber with N_2 and (m) opening the gate valve and removing the wafer.

Utilizing the apparatus and method of this invention the foregoing total process sequence removed about 1,000 Å of silicon dioxide over a period of less than two minutes. By maintaining chamber pressure in the 20-500 Torr range and a flow of the N_2 carrier at about 10 SLPM, the entire wafer is etched to a high degree of uniformity. Figure 6

which shows the remaining oxide thickness in angstroms at various locations across the wafer after the etch shows a uniformity of plus or minus 2% across the wafer when excluding the outer 0.25" edge of the wafer.

In the foregoing process the HF consumption was calculated, and it was found that the HF solution was depleted at a rate of 0.25-0.40 cc/min. at the optimum uniformity mass flow rate. At the etch rate of 20 Å/sec., the time required to strip 100 Å of oxide from the wafer was 5 seconds and in this time approximately 0.01 cc of HF was consumed. This indicates that approximately 20,000 six inch diameter wafers may be processed to remove 100 Å of silicon dioxide while using less than one liter of HF solution. This compares with the reported consumption rate of 500-750 liters per 10,000 wafers required in the current standard wet deck HF processing.

This invention not only reduces the required amount of chemicals but also avoids the disposal of any significant quantity of unused chemicals following the wafer processing.

Besides the HF oxide removal, the present method and apparatus includes a removal sequence for oxides/organics/metals using the following processing treatments:

1. Ozone treatment using mixture of $O_3/O/O_2$;
2. $HF-H_2O$;
3. H_2O in vapor state and/or liquid state for rinse;
4. $NH_3/O_3/H_2O$;
5. H_2O in vapor state and/or liquid state for rinse;
6. Hot N_2/Ar or isopropyl alcohol dry; and

7. Transfer wafer to reactor or cassette.

An alternative removal sequence to the sequence just previously described would include, after the second H_2O rinse in step No. 5, the treatment step of $HCl/O_3/H_2O$.

The treatment and processing apparatus 17 can be constructed similar to the processing housing shown in Fig. 7 which illustrates heating apparatus 135 at the wafer processing position and comprising a container 136 with front and back walls 137 and 138 located between a pair of reaction chambers 132, one of which is only partially shown. The reaction chamber 132 includes an outer wall 151 somewhat in the form of a hollow belljar, the larger open end of which is connected to the heating apparatus 135 around three sides thereof but open on the chamber 132 against one of the walls 137 and 138 of the heating apparatus. Inside the chamber member 151 is another chamber member 153 of similar shape, but smaller size providing a space between the members 151 and 153 for exhaust of reactant materials. Member 153 has a hollow cylindrical stem 154 which serves an as inlet for introducing reactant gases into the chamber member 153 in a direction toward the wafer 5 position at the larger opposite end of the chamber 153. A heat energy reflecting layer, film or foil surface 155, such as of gold or similar highly reflective metal film or infrared reflective film as beryllium oxide or titanium oxide, is provided on the inside surface of the chamber 153 other than in the stem 154 for reflecting heat energy from the heating apparatus 135 onto the front surface of the wafer S so that the temperature of the wafer S is maintained substantially uniform through its volume. A hollow cylindrical sleeve 156 is sealably connected to the end of chamber 151 remote from the location of the

wafer S and is connected by a flexible joint 157 to a flange 158 on the stem 154 of the inner chamber 153. A lateral outlet port 159 extends from the sleeve 156 and provides communication to the annular region between the sleeve 156 and the stem 154 which is in turn in communication with the space between the chambers 151 and 153.

Preferably the walls of the heating apparatus 135 are formed from materials with high conductive properties, such as solid silicon carbide. Such conductive surfaces are desired to permit maximum transfer of heat to the external surfaces of the walls 137 and 138 and to a wafer or semiconductor substrate S mounted thereon. The container 136 is substantially filled with a low melting point, high boiling point medium or material 133. For processing semiconductor substrates or wafers, the material 133 has a melting point below 350°C and a boiling point above 1000°C. The preferred material is essentially indium but bismuth and eutectic mixtures of indium and bismuth and other low melting point, high boiling point materials such as tin are also satisfactory.

At least one insulated resistive heating element (not shown) is positioned directly in the material 133 in the container 136. The heating element must be capable of generating high temperatures to melt the medium 133 and heat that medium 133 to a sufficiently high temperature without vaporizing the medium 133 so that a semiconductor wafer or substrate positioned in direct contact with the external surface of container walls 137 and 138 will be heated to the elevated temperature necessary to treat the wafer or substrate.

Processing gases can be introduced through the stem 154 into the interior of chamber 153 for direct application on the face of the wafer 5. Gases can be

exhausted from the region adjacent the face of wafer 5 through the space between chambers 151 and 153 and out the exhaust port 159. The flexible joint 157 allows movement of at least a portion of the outer chamber wall 151 on the port side of the heating apparatus 156 to open and close a region enabling the wafer to be inserted into the reaction chamber and positioned on the wall of the heater apparatus 135 and then removed from the reaction chamber after the appropriate processing step. The wafers can be transported to and from the reactor system in conventional carriers or cassettes and can actually move through a similarly configured chamber apparatus for cleaning (as described with reference to Figures 3 and 4) immediately prior to processing in the reaction chamber.

An alternative embodiment of the invention, similar to the embodiment of Fig. 7, is shown in Fig. 7A. In the embodiment of Fig. 7A an auxiliary heat source 161, such as an infrared lamp, is provided in the chamber 153 for directing heat energy onto the front surface of the wafer S. The stem 162 of the heat source 161 extends out of the inner chamber 153 through the stem 154 of the chamber 153. Heating the wafer from both the front and back insures uniform heating through the volume of the water thereby avoiding crystaline slip.

An alternative vapor-phase clean/etch reaction chamber 320 is shown in Fig. 8 which includes a schematic view of the overall process system. The material used to construct the chamber is a silicon carbide composite inert to essentially any reactant gas and is manufactured by Norton Company of Worchester, Massachusetts. The chamber 320 consists of two concentric spheres, 323 and 333 connected by a center ring or block 371 at which a wafer can be

inserted into the chamber. The diameter of the outer sphere 333 is approximately 24 centimeters and will accommodate one or two silicon wafers up to 150mm in diameter. The wafer is placed vertically in the chamber 320. The process gas can be injected in one side, either side or both sides of the chamber 320 and exhausted from either or both sides by a vacuum pump 340. Thus, a considerable amount of flexibility in gas phase dynamics is possible by controlling gas flows and vacuum supply. A heater, such as heater 135 shown in Figure 7, can be used to heat the wafer(s) up to 1,000°C.

Figure 8 also includes mass flow meters 341-344, gas sources feeding gas lines 345-348 and two vaporizers 351 and 352. Gas lines 353-356 from the vaporizers 351 and 352 and other gas sources are heated, as are the valves (not shown). All reactant transport components outside the reactor 320 are fabricated from teflon-based materials.

A typical sequence for cleaning or etching a device wafer is indicated in Figure 9. After insertion of the silicon wafer in the chamber, the door is clamped and the chamber evacuated to approximately one Torr in less than 10 seconds and preferably for at least one second which is indicated in Fig. 9 as step I. This first desorb step I tends to vaporize absorbed moisture and other volatile species, even from high aspect ratio trenches. Nitrogen or argon is then admitted to the system to about 350 Torr. Next, the cleaning or etching gas mixture of HF in H_2O flows through the chamber 320 in the carrier gas as designated in step II. After the prescribed cleaning or etching time, which is generally 10-60 seconds, the gas flows are stopped, and the chamber 320 is once more evacuated in less than 10 seconds to the milliTorr (10^{-3} Torr) range.

After a suitable pumping time, such as 20 to 30 seconds for desorption and evacuation of gases including reaction products, atmospheric pressure nitrogen or argon is readmitted to the chamber and the wafer removed for evaluation or additional processing. In certain cases the desorb step can extend upwards of 120 seconds and include application of heat to the wafer. All the above procedures are computer programmed and controlled.

To evaluate the vapor-phase clean/etch system and associated processing described with respect to Figs. 8 and 9, varying amounts of oxides were removed under selected process conditions, and the etch rates, etch uniformity and reproducibility of etching from run to run were determined. Typical results are shown in Figures 10A and 1-B. Figure 10A shows the thermal oxide thickness both before and after vapor-phase HF/H_2O etching and Figure 10B shows the total oxide etched. The processing conditions for arriving at 10A and 10B were the use of 25% HF in H_2O at 30°C, 9 l/min N_2, 250 Torr, 60 second etch time, 100mm dia. Si at 25°C. In Figure 10A oxide thickness data across a 100mm thermally oxidized wafer are shown before and after removing 1150 Å oxide. Differences in these two plots (the thickness of the oxide etched) are shown in Figure 10B. Total deviation of oxide etched for this example is ±1.3%. Other etching conditions were P_{vap} HF = 1.4 Torr, P_{vap} H_2O = 20 Torr, P_{total} = 250 Torr. Similar results were obtained for 125 and 150 mm diameter wafers and for various process conditions.

In Figure 11 thermal oxide removed or etched is plotted against the H_2O/HF exposure time. The etching conditions were 25% HF in H_2O at 50°C, 16 l/min N_2, 350 Torr, 150 mm dia. silicon wafers at 25°C. For these conditions an etch rate of 33.9 Å/second was

obtained. A slight offset along the time axis of Fig. 11 is discussed below. Other etch rate data have been obtained for varying HF/H_2O vapor pressures in range from 10 to 50 Å/sec.

Fig. 12 illustrates a similar plot showing etch characteristics of borophosphosilicate glass (BPSG). Boron and phosphorus concentrations were each approximately 5% by weight in this deposited oxide dielectric. Etch conditions for the BPSG were the same as those indicated with respect to Fig. 11. It is noted that the BPSG etch rate is approximately twice that of thermal oxides. This same ratio has been noted for etching BPSG oxides in conventional aqueous HF solutions.

While the mechanism of thermal oxide etch-removal in a HF/H_2O vapor mixtures is still being investigated, it is believed that the actual etching occurs by the action of a thin condensed layer of HF in H_2O on the oxide surface. This can explain the very good uniformity of etching and a lesser dependence on gas dynamics. It also helps to explain the importance of the operation at reduced pressure during the etch cycle and the final evacuation of the reaction chamber in removing reactants, reaction products, and contamination in a matter of seconds. The time offsets observed in Figs. 11 and 12 are probably due to the time required for this condensed film to form. Thus, the surface condition of the oxide plays an important role in the etching mechanism.

An important aspect of cleaning or removing native oxides on silicon with this invention prior to subsequent film deposition steps is to maintain the surface as free from oxide regrowth as possible. An investigation was carried out to monitor the effects of various ambients on native oxide regrowth of HF

vapor-etched silicon. This included wet and dry N_2 and O_2 and exposure to the light or the dark. The results were compared with room ambient exposure as well as treatment in aqueous HF solutions plus deionized water rinse. Oxide thicknesses were measured using a Gaertner Model No. L115B mapping ellipsometer.

Typical results of native oxide regrowth are presented in Figure 14. Data for 24-hour exposure of an HF vapor etched silicon surface to dry nitrogen and filtered room air are shown. The initial native oxide thickness was 12Å (as measured by the ellipsometer) while after HF vapor etch, it was 4Å. A thickness of 12Å was obtained after 24 hours in room air, while the dry N_2 exposure resulted in less than 7Å, or an increase of 1 to 2Å.

Auger electron spectroscopy analysis indicated relative carbon levels of 1.2Å after and aqueous HF etch followed by a dionized water rinse and 0.03 A after vapor HF/H_20 etch.

General observations of results obtained with regard to native oxide regrowth after vapor-phase HF etching of silicon indicate that (a) dry N_2 and O_2 give minimum regrowth; (b) a dark environment generally reduced oxide regrowth; (c) wet gases increase oxide regrowth 2 to 3 times; and (d) room air with relative humidity of 40% increases regrowth up to 10 times.

Contamination effects, both particulate and metallic, have been monitored on an on-going basis. It has been found that the vapor phase HF system tends to be very clean and does not add particles to the wafer. In a series of twelve runs where the native oxide was etched from the silicon surface, an average of 1.5 particles equal to or greater than 0.4 um were removed per run. Measurements were made with

a Tencor Model 5500 Surfscan particle analyzer. Average starting (pre-etch) counts were 9 particles ≥ 0.4 um per 150 mm wafer. Analysis indicates that no metallic impurities are added by the system. In fact, two separate evaluations indicated that Pb, Fe, Cu and Ni are typically reduced in concentration by more than 50% during native oxide removal by the HF vapor process. Pre-etch values were 0.5 to 1.0 x 10^{12} atoms/cm^2 as received from the supplier.

While a vapor phase cleaning system dealing primarily with HF/H_2O chemistry has been described, several other chemistries that are believed possible with this invention are gas phase analogs of conventional aqueous cleaning processes, such as ammonium hydroxide/hydrogen peroxide and hydrochloric acid/hydrogen peroxide.

The reactors 12, 13 and 17 of integrated assembly 10 can take the form of the housing 20 of Figs. 2 and 3, the apparatus 12 of Fig. 5, the apparatus 135 of Fig. 7 or the chamber 320 of Fig. 8 which are not only appropriate for cleaning chemistries but also ideally suited for the subsequent or in-situ chemical vapor deposition (CVD) of thin films, such as epitaxial and polycrystaline silicon, dielectrics, interconnect and contact metals and even regrowth of thermal oxides. Besides the integrated assembly 10 of Fig. 1 the cleaning and deposition process can be combined into one multichamber system, such as depicted in Fig. 15. In Fig. 15 a surface contamination removal module 412 is shown which is connected to an interprocess robot chamber 415. It is possible to move the clean wafer in vacuum through load locks 420 from module 412 to the next modules such as 413 and/or 417 for additional cleaning, native oxide regrowth or possible CVD without exposing the wafer to ambient

atmosphere. The adoption of sequential, in-situ processing, where the device wafer is not exposed to a reactive ambient between cleaning and subsequent processing, minimizes contamination and oxide regrowth and thus improves device performance, yield and reliability.

The terms and expressions which have been employed here are used as terms of description and not of limitations, and there is no intention, in the use of such terms and expressions, of excluding equivalents of the features shown and described, or portions thereof, it being recognized that various modifications are possible within the scope of the invention claimed.

CLAIMS

1. Semiconductor wafer processing apparatus comprising, in combination,

a processing housing having a substantially horizontal axis, means for supporting at least one wafer substantially vertically at a wafer treating position along said housing horizontal axis, a first housing member centered on said horizontal axis on one side of said wafer treating position, and means for introducing and directing a treatment medium into said first housing member in a direction substantially parallel to said horizontal axis and toward said wafer treating position.

2. The apparatus of claim 1 wherein said first housing member comprises a first inner cylindrical wall portion and a second outer cylindrical wall portion, said wall portions being coaxial and defining an inner cylindrical chamber for directing the treatment medium toward said wafer treating position and an outer annular chamber for directing the treatment medium away from said wafer treating position.

3. The apparatus of claim 1 including a second housing member centered on said horizontal axis on the other side of said wafer treating position and means for introducing and directing a treatment medium into said second housing member in a direction substantially parallel to said horizontal axis and toward said wafer treating position.

4. The apparatus of claim 3 wherein each of said first and second housing members comprises a first inner cylindrical wall portion and a second outer cylindrical wall portion, said wall portions being coaxial and defining an inner cylindrical chamber for directing the treatment medium toward said wafer treating position and an outer annular chamber for directing the treatment medium away from said wafer treating position.

5. The apparatus of claim 3 wherein said supporting means will support only a single wafer at said wafer treating position whereby one side of the single wafer will receive a treatment medium introduced into said first housing and the other side of the single wafer will receive a treatment medium introduced into said second housing.

6. The apparatus of claim 3 wherein said supporting means includes means for supporting a pair of wafers back to back whereby the front of one wafer will receive a treatment medium introduced into said first housing and the front of the other wafer will receive a treatment medium introduced into said second housing.

7. The apparatus of claim 6 wherein said supporting means includes a flat wall for heating at least one wafer by conduction and a heat transfer means comprising a low melting point, high boiling point metal contained within said supporting means in contact with said wall.

8. The apparatus of claim 1 wherein said introducing and directing means includes means for introducing a treatment medium in vapor phase.

9. The apparatus of claim 1 wherein said introducing and directing means includes means for introducing a treatment medium at very low to high velocity impingement upon the face of a wafer at said wafer treating position.

10. The apparatus of claim 1 including means for maintaining said first housing at subatmospheric pressure during introduction of said treatment medium.

11. The apparatus of claim 1 including means for reducing the pressure in said chamber to below 100 Torr before and after said treatment medium is introduced into said first chamber.

12. The apparatus of claim 11 wherein said pressure reducing means reduces the pressure in said first chamber to substantially 10^{-3} Torr before or after said medium is introduced into said first chamber.

13. The apparatus of claim 12 wherein said pressure is reduced to substantially 10^{-3} Torr before said medium is introduced into said first chamber.

14. The apparatus of claim 12 wherein said pressure is reduced to substantially 10^{-3} Torr after said medium is introduced into said first chamber.

15. The apparatus of claim 10 wherein said means for maintaining said first housing at subatmospheric pressure includes evacuation means for reducing the pressure in said first housing to a desorption pressure before and after introduction of

said treatment medium, said desorption pressure being substantially below said subatmospheric pressure during introduction of said treatment medium.

16. The apparatus of claim 15 wherein said evacuation means reduces the pressure in said first chamber to substantially 10^{-3} Torr before or after said medium is introduced into said first chamber.

17. The apparatus of claim 16 wherein said pressure is reduced to substantially 10^{-3} Torr before said medium is introduced into said first chamber.

18. The apparatus of claim 16 wherein said pressure is reduced to substantially 10^{-3} Torr after said medium is introduced into said first chamber.

19. The apparatus of claim 1 including means for maintaining said first housing at superatmospheric pressure during introduction of said treatment medium.

20. The apparatus of claim 1 including means for introducing radiation into said first housing.

21. The apparatus of claim 1 including means for automatically moving a wafer into and out of said housing.

22. The apparatus of claim 13 including means for automatically moving a wafer from said housing to another wafer treating apparatus.

23. The apparatus of claim 1 including another wafer treating apparatus having a second processing housing, said processing housing and said second

processing housing being integral and means for moving a wafer from said processing housing to said second processing housing without exposing the wafer to ambient atmosphere.

24. Semiconductor wafer processing apparatus comprising, in combination,

a processing housing having a substantially horizontal axis, means for supporting at least one wafer substantially vertically at a wafer treating position along said housing horizontal axis, a first housing member centered on said horizontal axis on one side of said wafer treating position, means for introducing and directing a treatment medium into said first housing member in a direction substantially parallel to said horizontal axis and toward said wafer treating position, a second housing member centered on said horizontal axis on the other side of said wafer treating position and means for introducing and directing a treatment medium into said second housing member in a direction substantially parallel to said horizontal axis and toward said wafer treating position, each of said first and second housing members comprising a first inner cylindrical wall portion and a second outer cylindrical wall portion, said wall portions being coaxial and defining an inner cylindrical chamber for directing the treatment medium toward said wafer treating position and an outer annular chamber for directing the treatment medium away from said wafer treating position.

25. The apparatus of claim 24 wherein said supporting means will support only a single wafer at

said wafer treating position whereby one side of the single wafer will receive a treatment medium introduced into said first housing and the other side of the single wafer will receive a treatment medium introduced into said second housing.

26. The apparatus of claim 24 wherein said supporting means will support a pair of wafers back to back whereby the front of one wafer will receive a treatment medium introduced into said first housing and the front of the other wafer will receive a treatment medium introduced into said second housing.

27. The apparatus of claim 26 wherein said supporting means includes a flat wall for heating at least one wafer by conduction and a heat transfer means comprising a low melting point, high boiling point metal contained within said supporting means in contact with said wall.

28. The apparatus of claim 24 wherein said introducing and directing means includes means for introducing a treatment medium in vapor phase.

29. The apparatus of claim 24 wherein said introducing and directing means includes means for introducing a treatment medium for very low to high velocity impingement upon the face of a wafer at said wafer treating position.

30. The apparatus of claim 24 including means for maintaining at least said first housing at subatmospheric pressure during introduction of said treatment medium.

31. The apparatus of claim 24 including means for reducing the pressure in said chamber to below 100 Torr before and after said treatment medium is introduced into said first chamber.

32. The apparatus of claim 31 wherein said pressure reducing means reduces the pressure in said first chamber to substantially 10^{-3} Torr before or after said medium is introduced into said first chamber.

33. The apparatus of claim 32 wherein said pressure is reduced to substantially 10^{-3} Torr before said medium is introduced into said first chamber.

34. The apparatus of claim 32 wherein said pressure is reduced to substantially 10^{-3} Torr after said medium is introduced into said first chamber.

35. The apparatus of claim 30 wherein said means for maintaining said first housing at subatmospheric pressure includes evacuation means for reducing the pressure in said first housing to a desorption pressure before and after introduction of said treatment medium, said desorption pressure being substantially below said subatmospheric pressure during introduction of said treatment medium.

36. The apparatus of claim 35 wherein said evacuation means reduces the pressure in said first chamber to substantially 10^{-3} Torr before or after said medium is introduced into said first chamber.

37. The apparatus of claim 36 wherein said pressure is reduced to substantially 10^{-3} Torr before said medium is introduced into said first chamber.

38. The apparatus of claim 36 wherein said pressure is reduced to substantially 10^{-3} Torr after said medium is introduced into said first chamber.

39. The apparatus of claim 24 including means for maintaining at least said first housing at superatmospheric pressure during introduction of said treatment medium.

40. The apparatus of claim 24 including means for introducing radiation into at least said first housing.

41. The apparatus of claim 24 including means for automatically moving a wafer into and out of said housing.

42. The apparatus of claim 41 including means for automatically moving a wafer from said housing to another wafer treating apparatus.

43. The apparatus of claim 24 including another wafer treating apparatus having a second processing housing, said processing housing and said second processing housing being integral and means for moving a wafer from said processing housing to said second processing housing without exposing the wafer to ambient atmosphere.

44. The method of treating a semiconductor wafer comprising the steps of:

positioning the wafer substantially vertically,

directing a treatment medium substantially horizontally against at least one face of the wafer, and
withdrawing the treatment medium away from said one face of said wafer substantially coaxially and outwardly from the medium being directed against said face of the wafer.

45. The method of processing semiconductor wafers comprising the steps of:
positioning a wafer in a first chamber,
exposing at least a first surface of the wafer in the first chamber to a first gaseous medium for removing material from said first surface of said wafer,
clearing said first gaseous medium from said first chamber, and
exposing said first surface of said wafer to a second gaseous medium for depositing material onto said first surface of said wafer without exposing said wafer to ambient atmosphere.

46. The method of claim 45 wherein said step of exposing said wafer to a second gaseous medium comprises exposing said wafer to said second gaseous medium in said first chamber.

47. The method of claim 45 including after said step of exposing said wafer to a first gaseous medium and before the step of exposing said wafer to said second gaseous medium the step of moving said wafer from said first chamber to a second chamber without exposing said wafer to ambient atmosphere.

48. The apparatus for processing semiconductor wafers comprising the steps of:

a first chamber,

means for positioning a wafer in said first chamber,

first means for exposing at least a first surface of the wafer in said first chamber to a first gaseous medium for removing material from said first surface of said wafer,

means for clearing said first gaseous medium from said first chamber, and

second means for exposing said first surface of said wafer to a second gaseous medium for depositing material onto said first surface of said wafer without exposing said wafer to ambient atmosphere.

49. The apparatus of claim 48 wherein said second exposing means comprises means for exposing said wafer to said second gaseous medium in said first chamber.

50. The apparatus of claim 48 including a second chamber and wherein said second exposing means includes means for exposing said wafer to said second gaseous medium in said second chamber and means for moving said wafer from said first chamber to said second chamber without exposing said wafer to ambient atmosphere.

51. The method of processing semiconductor wafers comprising the steps of:

positioning a wafer in a first chamber,

reducing the pressure within said first chamber,

exposing at least a first surface of said wafer to a first gaseous medium in said first chamber for removing material from said first surface of said wafer, and then evacuating said first chamber.

52. The method of claim 51 wherein said step of reducing the pressure within said first chamber comprises reducing the pressure to at least substantially one Torr.

53. The method of claims 51 or 52 wherein said step of evacuating said first chamber comprises the step of evacuating said first chamber to at least substantially 10^{-3} Torr.

54. The method of processing semiconductor wafers comprising the steps of:

pressurizing a first chamber with an inert gas to a positive pressure,
loading and positioning a wafer in said first chamber,
evacuating said first chamber,
exposing at least a first surface of said wafer to a first gaseous medium in said first chamber,
evacuating said first chamber, and
back filling said first chamber with inert gas.

55. The method of claim 54 wherein said step of reducing the pressure within said first chamber comprises reducing the pressure to at least substantially one Torr.

56. The method of claims 54 or 55 wherein said step of evacuating said first chamber comprises the step of evacuating said first chamber to at least substantially 10^{-3} Torr.

57. The apparatus for processing semiconductor wafers comprising:

a chamber,

means for pressurizing said chamber with an inert gas to a positive pressure,

means for loading and positioning a wafer in said chamber,

means for evacuating said chamber,

means for exposing at least a first surface of said wafer to a first gaseous medium in said chamber, and

means for again evacuating said chamber.

58. The method of etching surface of a semiconductor wafer comprising the steps of:

pressurizing a first chamber with an inert gas to a positive pressure, loading and positioning the wafer in said first chamber, evacuating said first chamber to substantially one Torr, exposing at least a first surface of said wafer to gaseous hydrogen fluoride and water at subatmospheric pressure,

evacuating said first chamber at least to substantially 10^{-3} Torr.

59. The apparatus of claim 7 or 27 including means for directing auxiliary heat to the front side of said one wafer.

60. The apparatus of claim 59 wherein said means for directing auxiliary heat to the front side of said one wafer includes means on the inside surface of said container for reflecting heat energy onto the front side of said wafer.

61. The apparatus of claim 59 wherein said means for directing auxiliary heat to the front side of said wafer includes an auxiliary heat source in said reaction chamber.

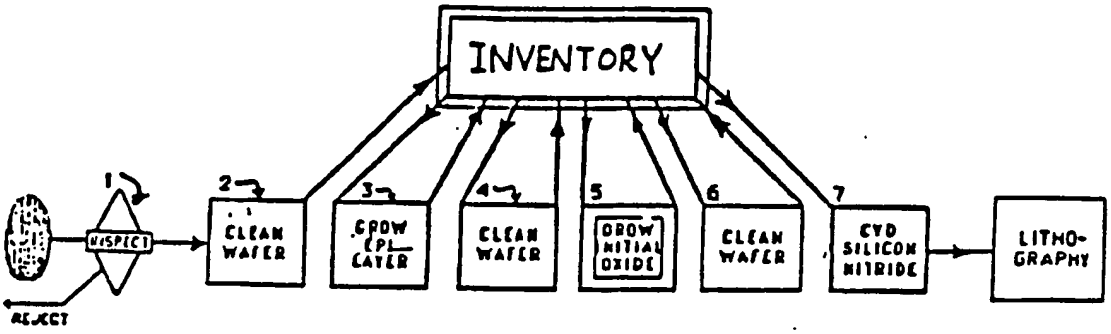

FIG. 1 PRIOR ART

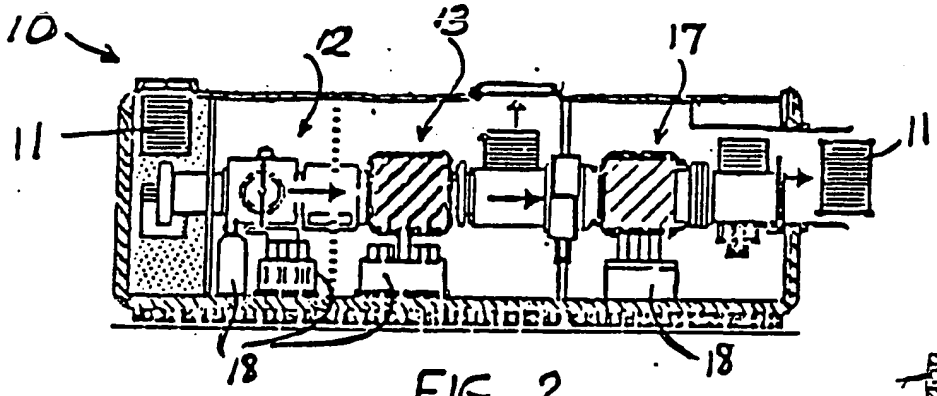

FIG. 2

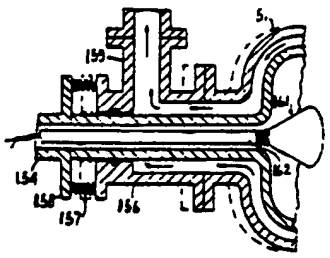

FIG. 7A

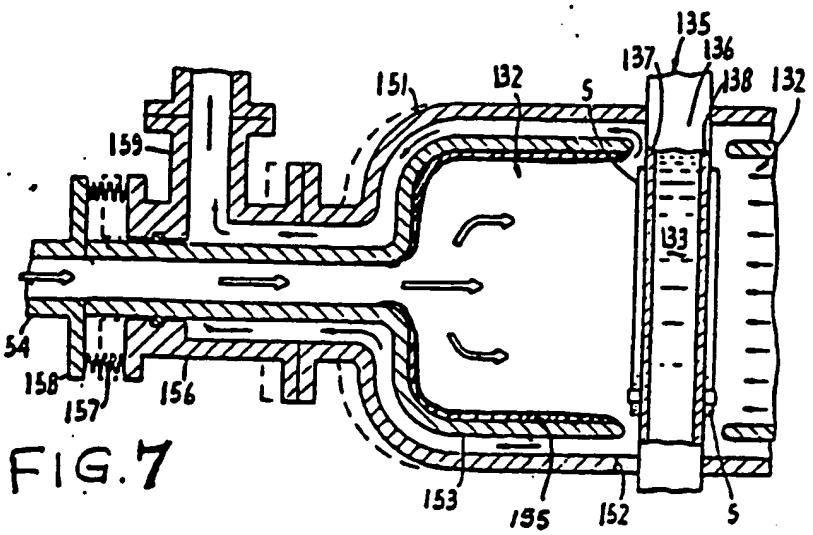

FIG. 7

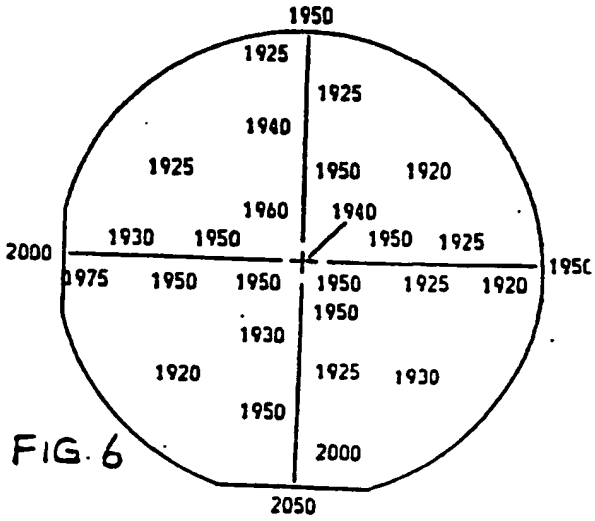

FIG. 6

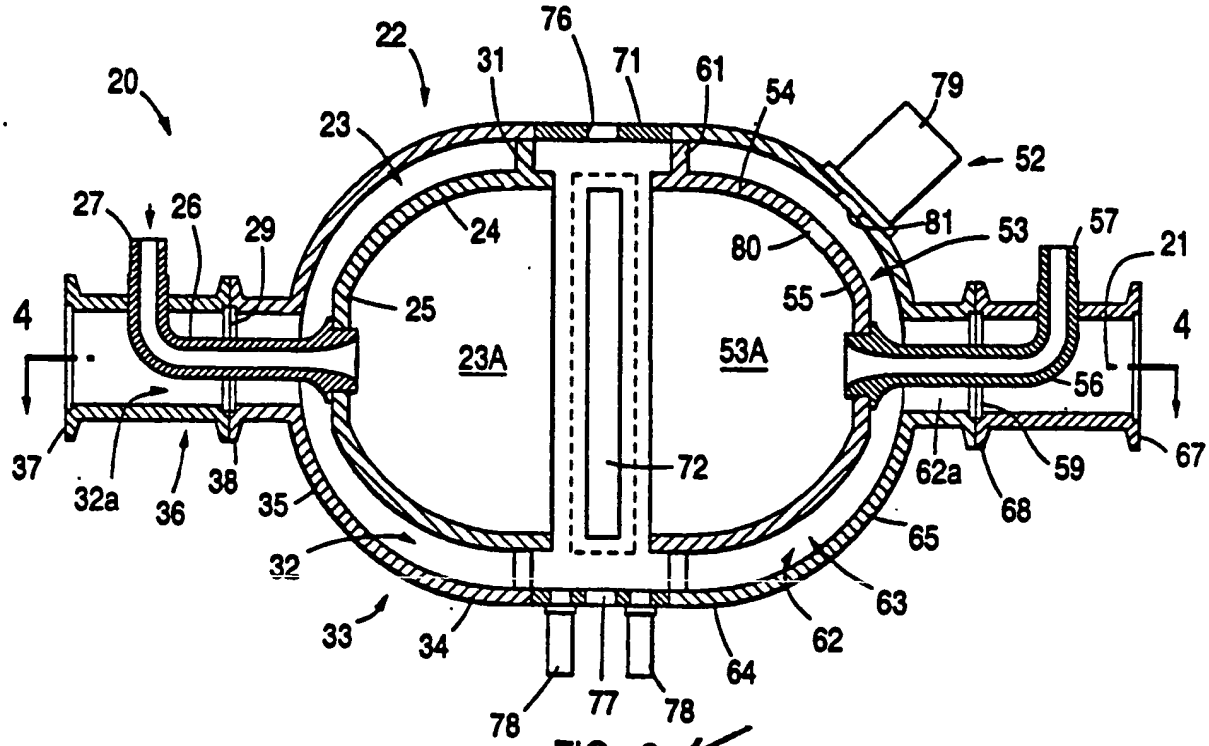

FIG. 3

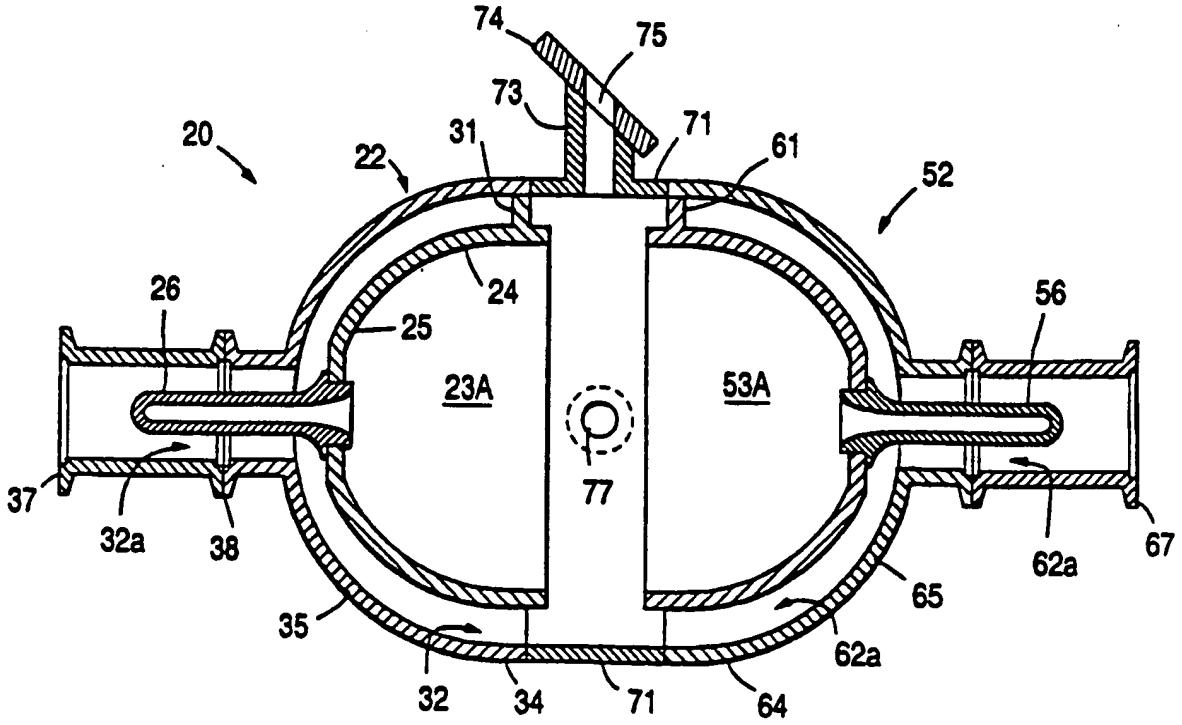

FIG. 4

SUBSTITUTE SHEET

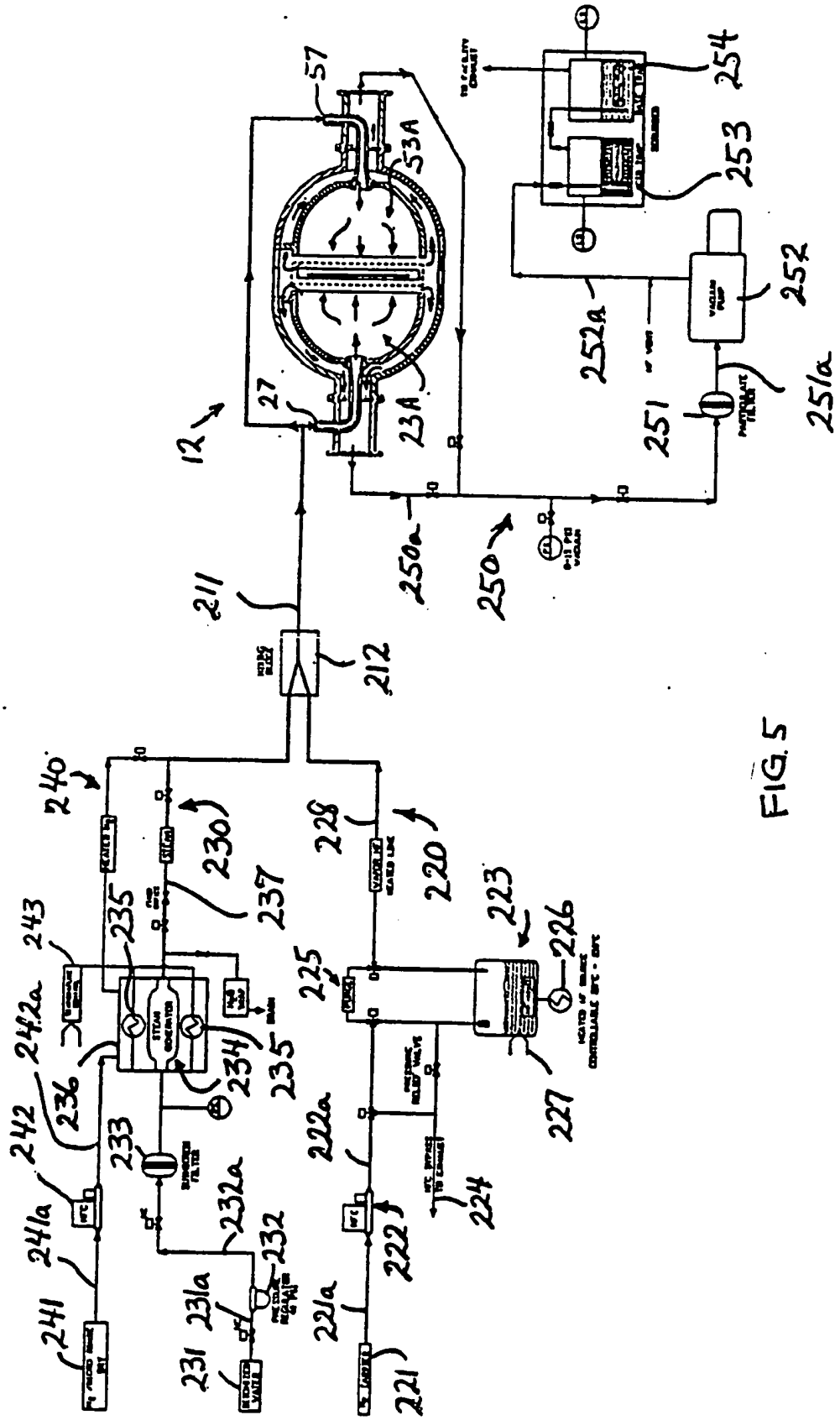
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FIG. 5

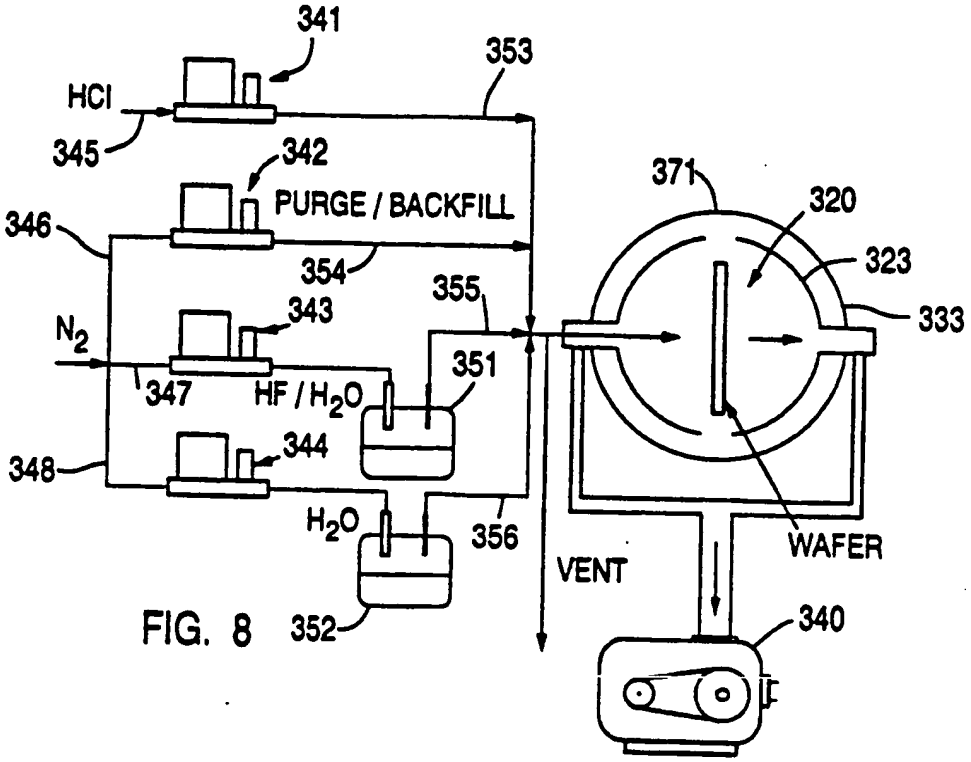

FIG. 8

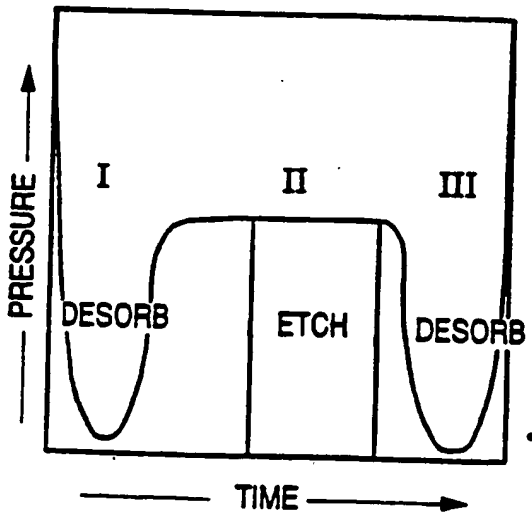

FIG. 9

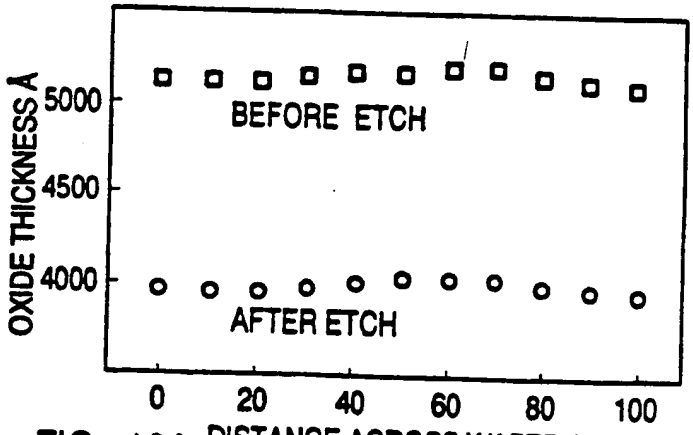

FIG. 10A

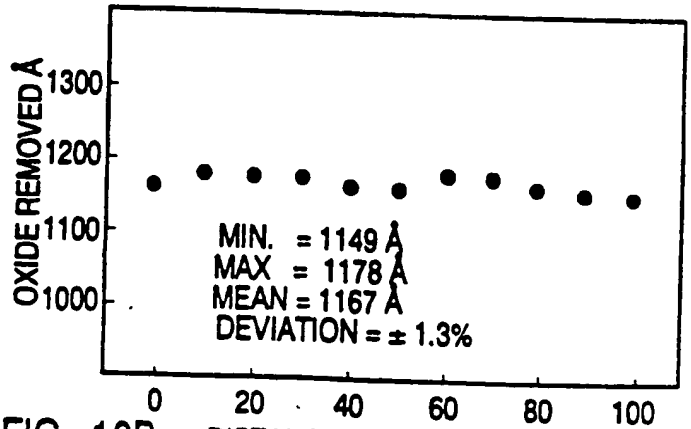

FIG. 10B

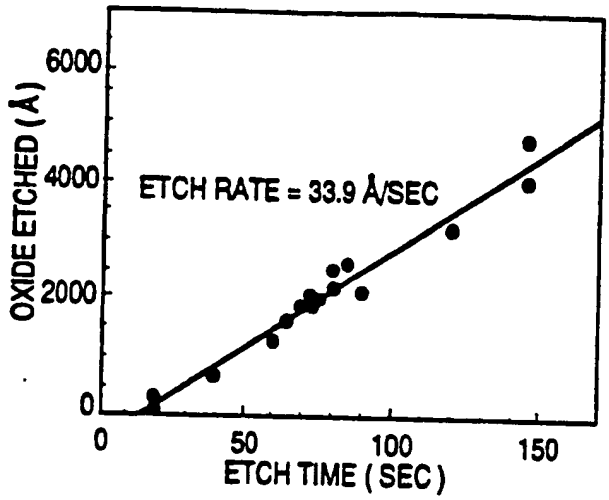

FIG. 11

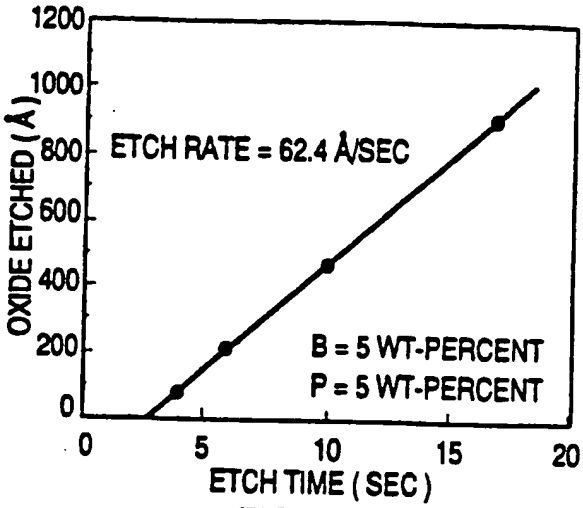

FIG. 12

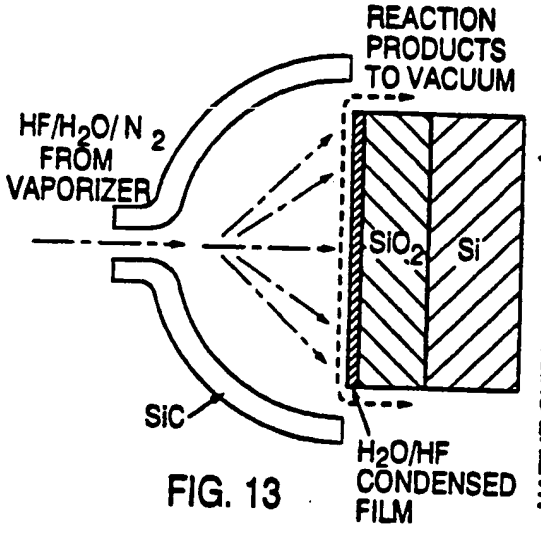

FIG. 13

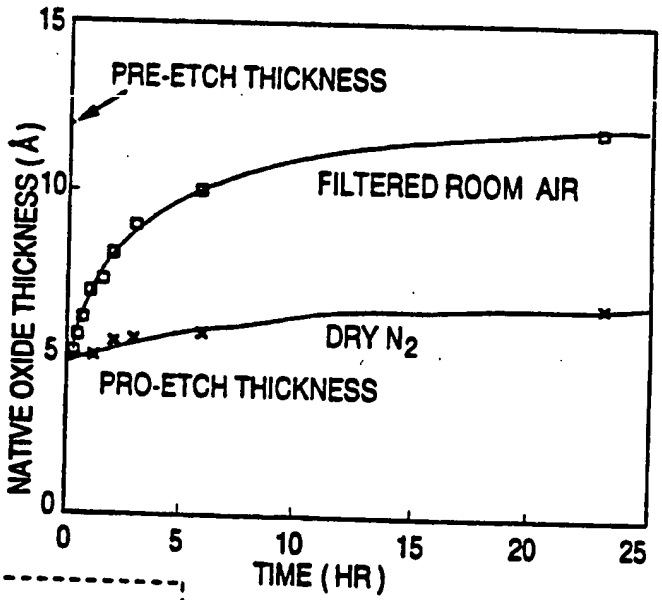

FIG. 14

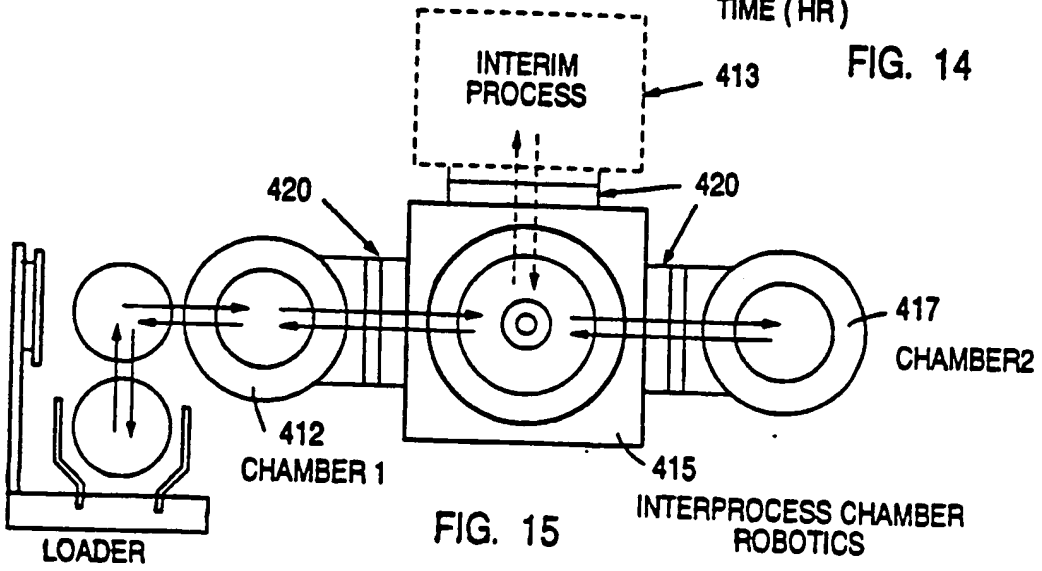

FIG. 15

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US89/04592

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(4): C23C 16/44
U.S.CL.: 118/719; 427/248.1

II FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
U.S.	15/330, 345; 118/500, 715, 719, 725, 728; 134/25.1 25.4, 31, 37, 42; 156/345, 646; 219/390, 460, 462 530, 540; 427/248.1, 255.5

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	US, A, 4,668,365 (FOSTER ET AL.) 26 May 1987, see Figure 4; col. 4, lines 43-52; col. 7, lines 1-6; col. 9, lines 12-47; col. 10, lines 1-3, 25-37, and 62-67; col. 11, lines 22-34.	1,3,5-18, 44-46,48, 49,51-53 57,58
Y	US, A, 4,609,428 (FUJIMURA) 02 September 1986, see Figure 2a; col. 5, lines 43-49; col. 7, lines 7-28 and 47-68; col. 8, lines 1-2.	1,8,9,11-18,20,57
Y	US, A, 4,659,401 (REIF ET AL.) 21 April 1987, see Figure 1; col. 4, lines 28-35 and 41-44.	2,10-18
Y	US, A, 4,605,479 (FAITH, JR.) 12 August 1986, see Figure; col. 2, line 63- col. 4, line 22.	23,48,50, 51-56

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

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IV. CERTIFICATION

Date of the Actual Completion of the International Search

20 November 1989

Date of Mailing of this International Search Report

21 DEC 1989

International Searching Authority

ISA/US

Signature of Authorized Officer

TERRY J. OWENS

Form PCT/ISA/210 (second sheet) (Rev.11-87)

III DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
Y	US, A, 4,401,507 (ENGLE) 30 August 1983, see Figure 1; col. 2, lines 39-40 and 51-58; col. 3, lines 43-48; col. 4, lines 14-17.	45,46,48 49,51,52
Y	US, A, 4,402,997 (HOGAN ET AL.) 06 September 1983, see Figure 1; col. 2, lines 33-40 and 45-64; col. 3, lines 1-11.	57
P &	US, A, 4,778,559 (McNEILLY) 18 October 1988, see Figure 10; col. 7, line 44- col. 8, line 24; claim 23.	1-9, 21, 24 26-29, 44, 48-50